AN3142
Application note

Solution for designing a 400 W fixed-off-time controlled PFC preregulator with the L6563S and L6563H

Introduction

In addition to the transition mode (TM) and fixed-frequency continuous conduction mode (FF-CCM) operation of PFC preregulators, a third approach is proposed that couples the simplicity and affordability of TM operation with the high-current capability of FF-CCM operation. This solution is a peak current-mode control with fixed-off-time (FOT). Design equations are given and a practical design for a 400 W board is illustrated and evaluated.

Two methods of controlling power factor corrector (PFC) preregulators based on boost topology are currently in use: the fixed-frequency (FF) PWM and the transition mode (TM) PWM (fixed on-time, variable frequency). The first method employs average current-mode control, a relatively complex technique requiring sophisticated controller ICs (e.g. the L4981A/B from STMicroelectronics) and a considerable component count. The second uses the simpler peak current-mode control, which is implemented with cheaper controller ICs (e.g. the L6561, L6562, L6562A and L6563S from STMicroelectronics), and far fewer external parts, therefore it is far less expensive. In the first method the boost inductor works in continuous conduction mode (CCM), while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given power throughput, TM operation involves higher peak currents as compared to FF-CCM (*Figure 1* and *Figure 2*).

Figure 1. Line, inductor, switch and diode currents in FF-CCM PFC

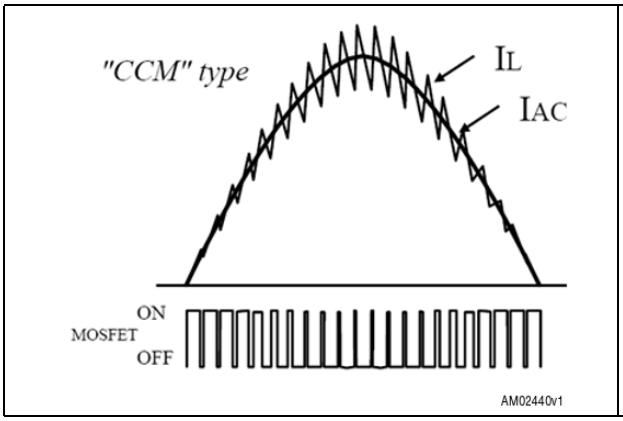
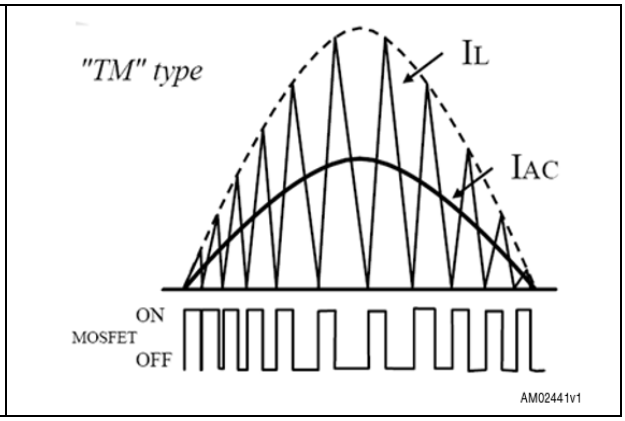


Figure 2. Line, inductor, switch and diode currents in TM PFC



This demonstration, consistent with the above mentioned cost considerations, suggests the use of TM in a lower power range, while FF-CCM is recommended for higher power levels.

This criterion, though always true, is sometimes difficult to apply, especially for a midrange power level, around 150-300 W. The assessment of which approach gives the better cost/performance trade-off needs to be done on a case-by-case basis, considering the cost and the stress of not only power semiconductors and magnetic but also of the EMI filter. At the same power level, the switching frequency component to be filtered out in a TM system is twice the line current, whereas it is typically 1/3 or 1/4 in a CCM system.

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1 Introduction to FOT control

In this area where the TM/CCM usability boundary is uncertain, a third approach that couples the simplicity and affordability of TM operation with the high-current capability of CCM operation may be a solution to the dilemma. Generally speaking, FF PWM is not the only alternative when CCM operation is desired. FF PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter operates in either CCM or DCM depending on the input voltage and the loading conditions. Exactly the same result can be achieved if the on-time only is modulated and the off-time is kept constant, in which case, however, the switching frequency is no longer fixed (*Figure 3* and *Figure 4*). This is referred to as “fixed-off-time” (FOT) control. Peak-current-mode control can still be used.

Figure 3. Basic waveforms for fixed frequency PWM

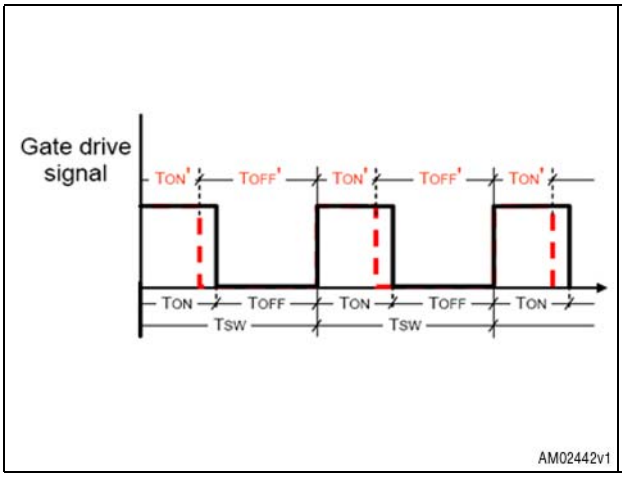
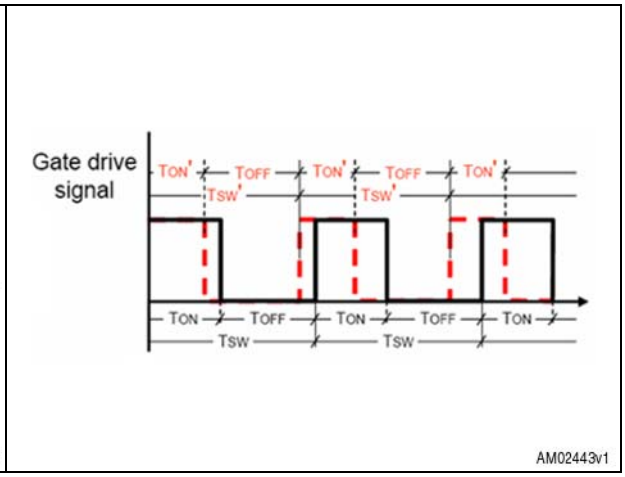


Figure 4. Basic waveforms for fixed-off-time PWM

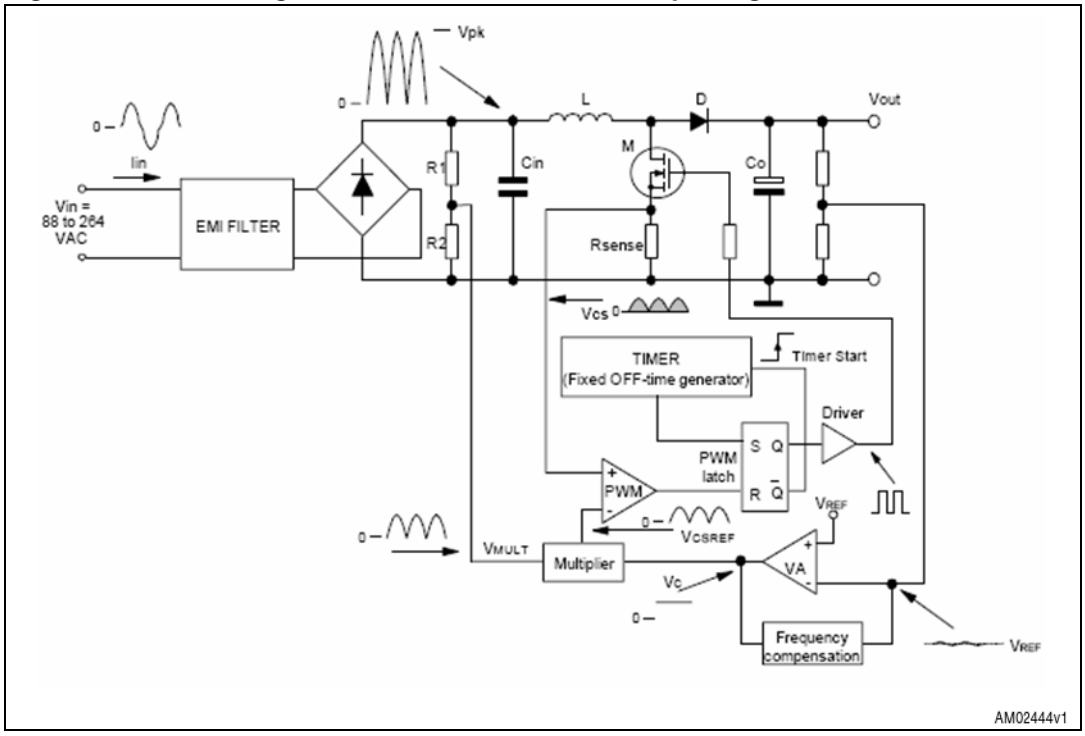


An important factor is that FOT control does not need a specialized control IC. A simple modification of a standard TM PFC controller operation, requiring just a few additional passive parts and no significant extra cost, is all that is needed.

2 Operation of an FOT-controlled PFC preregulator

Figure 5 shows a block diagram of an FOT-controlled PFC preregulator. An error amplifier (VA) compares a portion of the preregulator's output voltage Vout with a reference VREF and generates an error signal V_C proportional to their difference. V_C, a DC voltage by hypothesis, is fed into an input of the multiplier block and multiplied by a portion of the rectified input voltage V_{MULT}. At the output of the multiplier, there is a rectified sinusoid, V_{CSREF}, which has an amplitude proportional to that of V_{MULT} and to V_C, which represents the sinusoidal reference for PWM modulation. V_{CSREF} is fed into the inverting input of a comparator that, on the non-inverting input, receives the voltage V_{CS} on the sense resistor R_{sense}, proportional to the current flowing through switch M (typically a MOSFET) and the L inductor during the on-time of M. When the two voltages are equal, the comparator resets the PWM latch and M, supposedly already ON, is switched OFF.

Figure 5. Block diagram of an FOT-controlled PFC pre-regulator

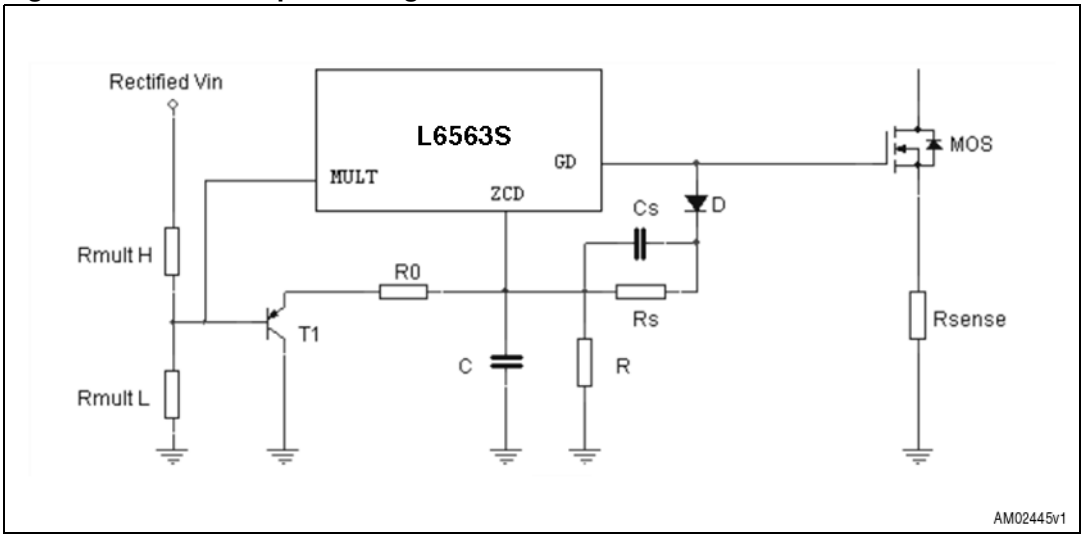


As a result, V_{CSREF} determines the peak current through the M and the L inductor. As V_{CSREF} is a rectified sinusoid, the inductor peak current is also enveloped by a rectified sinusoid. The line current Iin is the average inductor current that is the low-frequency component of the inductor current resulting from the low-pass filtering operated by the EMI filter. The PWM latch output Q going high activates the timer that, after a predetermined time in which T_{OFF} has elapsed, sets the PWM latch, therefore turning M on and starting another switching cycle. If T_{OFF} is such that the inductor current does not fall to zero, the system operates in CCM. It is apparent that FOT control requires almost the same architecture as TM control, just the way the off-time of M is determined also changes. It is not a difficult task to modify externally the operation of the standard TM PFC controller so that the off-time of M is fixed. As a controller we refer to the L6563S [*4*], which is suitable for power applications of a few hundred watts because of its gate drive capability and its high noise immunity. For a more detailed and complex description of the fixed off-time technique and in particular the line modulated FOT, please refer to [*5*].

3 The circuit implementing the line-modulated fixed-off-time with the new L6563S

The circuit that implements LM-FOT control with the L6563S is shown in *Figure 6*. During the on-time of the MOSFET the gate voltage V_{GD} = 15 V is high, the D diode is forward biased and the voltage at the ZCD pin is internally clamped at $V_{ZCDclamp}$ 5.7 V. During the off-time of M V_{GD} = 10 V is low, the D diode is reverse-biased and the voltage at the pin decays with an exponential law until it reaches the triggering threshold ($V_{ZCDtrigger}$ 0.7 V) that causes the switch to turn on. The time needed for the ZCD voltage to go from $V_{ZCDclamp}$ to $V_{ZCDtrigger}$ defines the duration of the off-time T_{OFF}.

Figure 6. Circuit implementing FOT control with the L6563S



The circuit in *Figure 6*. makes T_{OFF} a function of the RMS line voltage thanks to the peak holding effect of T1 (which acts as a buffer) along with R and C whose time constant is significantly longer than a line half-cycle. With the addition of R0 and T1, as long as the voltage on the ZCD pin during T_{OFF} is above $V_{mult}+V_{BE}$, C is discharged through R and R0, following the law:

Equation 1

$$V'_{ZCD}(t) = \left[V_{ZCDclamp} - \frac{R}{R_0 + R} \cdot (V_{mult} + V_{BE}) \right] \cdot e^{-\frac{t \cdot (R+R_0)}{(RR_0) \cdot C}} + \frac{R}{R_0 + R} \cdot (V_{mult} + V_{BE})$$

As $V'_{ZCD}(t)$ falls below $V_{mult}+V_{BE}$, T1 is cut off and C is discharged through R only, so that its evolution from that point on is described by:

Equation 2

$$V''_{ZCD}(t) = \frac{R}{R_0 + R} \cdot (V_{mult} + V_{BE}) \cdot e^{-\frac{t}{R \cdot C}}$$

$V'_{ZCD}(t)$ decreases from $V_{ZCDclamp}$ = 5.7 V to $V_{mult}+V_{BE}$ in the following time period t':

Equation 3

$$t' = -\frac{R \cdot R_0}{R + R_0} \cdot C \cdot \ln\left[\frac{(V_{mult} + V_{BE}) \cdot R_0}{V_{ZCDclamp} \cdot (R + R_0) - (V_{mult} + V_{BE}) \cdot R}\right]$$

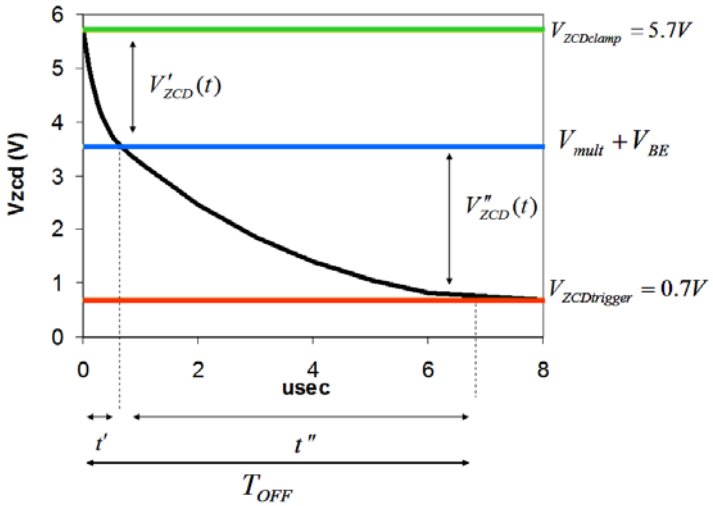
and $V''_{ZCD}(t)$ decreases from $V_{mult}+V_{BE}$ to $V_{ZCDtrigger}$ = 0.7 V level in the following time period t'':

Equation 4

$$t'' = -RC \cdot \ln\left[\frac{V_{ZCDtrigger}}{V_{mult} + V_{BE}}\right]$$

Figure 7 illustrates the signal on the ZCD pin with the two discharging time constants depending on the two resistors R, R0 and the L6563S parameters, particularly the upper clamp voltage and the triggering voltage of the ZCD pin.

Figure 7. ZCD pin signal with the fixed off-time generator circuit



The sum of the two time periods is the off-time function:

Equation 5

$$T_{OFF} = -RC \cdot \left[\frac{R_0}{R + R_0} \cdot \ln\left[\frac{(V_{mult} + V_{BE}) \cdot R_0}{V_{ZCDclamp} \cdot (R + R_0) - (V_{mult} + V_{BE}) \cdot R}\right] + \ln\left(\frac{V_{ZCDtrigger}}{(V_{mult} + V_{BE})}\right)\right]$$

In this way, once the multiplier operating point (that is, the V_{mult} / VAC ratio) is fixed, with a proper selection of R and R0 it is possible to increase T_{OFF} with the line voltage so that, at maximum line voltage, it is always $T_{ON}>T_{ONmin}$ = 450 ns for the L6563S [4]. This is a condition needed in order to avoid line distortion [5].

It is easy to see that T_{OFF} is now a function of the instantaneous line voltage. We refer to this technique as “line-modulated fixed-off-time” (LM-FOT) [5].

This modification, though simple, introduces profound changes in the timing relationships, with a positive influence on the energetic relationships. From the control point of view, modulating T_{OFF} is a feedforward term that modifies the gain but does not change its characteristics. Consequently, all of the properties of the standard FOT control are maintained. Due to the highly non-linear nature of the T_{OFF} modulation introduced by T1 and R0, its effects are discussed only qualitatively and the quantitative aspects are provided graphically for a specific case in [5].

As a practical rule, it is convenient to first select a capacitor and then to calculate the resistor needed to achieve the desired T_{OFF} (see *Section 4.3.7 on page 20*).

As the gate voltage V_{GD} goes high, the Rs resistor charges the timing capacitor C as quickly as possible up to $V_{ZCDclamp}$, without exceeding clamp rating (I_{ZCDx} =10 mA). Then it must fulfill the following inequalities:

Equation 6

$$\frac{V_{GDx} - V_{ZCDclamp} - V_F}{I_{ZCDx} + \frac{V_{ZCDclamp}}{R}} < Rs < R \cdot \frac{V_{GD} - V_{ZCDclamp} - V_F}{V_{ZCDclamp}}$$

where V_{GD} (assume V_{GD} = 10 V) is the voltage delivered by the gate driver, V_{GDx} = 15 V its maximum value, and VF the forward drop on D.

When working at high line/light load the on-time of the power switch becomes very short and the Rs resistor alone is no longer able to charge C up to $V_{ZCDclamp}$. The speed-up capacitor Cs is then used in parallel to Rs. This capacitor causes an almost instantaneous charge of C up to a level, after that Rs completes the charge up to $V_{ZCDclamp}$. It is important that the steep edge caused by Cs does not reach the clamp level, otherwise the internal clamp of the L6563S undergoes uncontrolled current spikes (limited only by the dynamic resistance of the 1N4148 and the ESR of Cs) that could overstress the IC. Cs must then be:

Equation 7

$$Cs < C \frac{V_{ZCDclamp}}{V_{GDx} - V_{ZCDclamp} - V_F}$$

4 Designing a fixed-off-time PFC

4.1 Input specification

This first part is a detailed specification of the operating conditions of the circuit that is needed for the following calculations in *Section 4.2 on page 11*. In this example a 400 W, wide input range mains PFC circuit has been considered. Some design criteria are also given.

- Mains voltage range (VAC rms): $VAC_{min} = 90Vac$ $VAC_{max} = 265Vac$ (1)
- Minimum mains frequency: $f_l = 47Hz$ (2)
- Rated output power (W): $P_{out} = 400W$ (3)

Because the PFC is a boost topology, the regulated output voltage depends strongly on the maximum AC input voltage. In fact, for correct boost operation the output voltage must always be higher than the input and therefore, because Vin max is V_{pk}, the output has been set at 400 Vdc as the typical value. If the input voltage is higher, as typical in ballast applications, the output voltage must be set higher accordingly. As a rule of thumb the output voltage must be set 6/7% higher than the maximum input voltage peak.

- Regulated DC output voltage (Vdc) $V_{out} = 400V$ (4)

The target efficiency and PF are set here at minimum input voltage and maximum load. They are used for the following operating condition calculation of the PFC. Of course at high input voltage the efficiency is higher.

- Expected efficiency (%): $\eta = \frac{P_{out}}{P_{in}} = 90\%$ (5)
- Expected power factor: $PF = 0.99$ (6)

Because of the narrow loop voltage bandwidth, the PFC output can face overvoltages at startup or in case of load transients. To protect from excessive output voltage that can overstress the output components and the load, in the L6563S a device pin (PFC_OK, pin #6) has been dedicated to monitor the output voltage with a separate resistor divider, selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (Vovp), usually larger than the maximum Vout that can be expected, also including worst-case load/line transients.

- Maximum. output voltage (Vdc): $V_{OVP} = 430V$ (7)

The mains frequency generates a $2f_L$ voltage ripple on the output voltage at full load. The ripple amplitude determines the current flowing into the output capacitor and the ESR. Additionally, a certain holdup capability in case of mains dips can be requested from the PFC in which case the output capacitor must also be dimensioned, taking into account the required minimum voltage value ($V_{out\,min}$) after the elapsed holdup time (t_{Hold}).

- Maximum output low frequency ripple: $\Delta V_{out} = 10V$ (8)

- Minimum output voltage after line drop (Vdc): $V_{out\,min} = 300V$ (9)

- Holdup capability (ms): $t_{Hold} = 20ms$ (10)

The PFC minimum switching frequency is one of the main parameters used to dimension the boost inductor. Here we consider the switching frequency at low mains on the top of the sinusoid and at full load conditions. As a rule of thumb, it must be higher than the audio bandwidth in order to avoid audible noise and additionally it must not interfere with the L6563S minimum internal starter period, as given in the datasheet. On the other hand, if the minimum frequency is set too high the circuit shows excessive losses at higher input voltage and probably operates skipping switching cycles not only at light load. Typical minimum frequency range is 55-95 kHz for wide range operation.

- Minimum switching frequency (kHz) $f_{sw\,min} = 80kHz$ (11)

Where f_{swmin} = 1/(T+220 nsec) due to the ZCD - gate drive signal delay typical of the L6563S.

The design is to be done on the basis of a ripple factor (the ratio of the maximum current ripple amplitude to the inductor peak current at minimum line voltage) kr=0.34.

- Ripple factor $k_r = 0.34$ (12)

In order to properly select the power components of the PFC and dimension the heat sinks in case they are needed, the maximum operating ambient temperature around the PFC circuitry must be known. Please note that this is not the maximum external operating temperature of the entire equipment, but it is the local temperature at which the PFC components are working.

- Maximum ambient temperature (°C): $T_{ambx} = 50°C$ (13)

4.2 Operating condition

The first step is to define the main parameters of the circuit, using the specification points given in *Section 4.1 on page 9*:

Rated DC output current:

Equation 8

$$I_{out} = \frac{P_{out}}{V_{out}} \quad I_{out} = \frac{400W}{400V} = 1.00A$$

Maximum input power:

Equation 9

$$P_{in} = \frac{P_{out}}{\eta} \quad P_{in} = \frac{400W}{90} \cdot 100 = 444.44W$$

Referring to the main currents shown in *Figure 1*, the following formula expresses the maximum value of current circulating in the boost cell which means at minimum line voltage of the selected range:

RMS input current:

Equation 10

$$I_{in} = \frac{P_{out}}{VAC_{min} \cdot PF} \quad I_{in} = \frac{400W}{90Vac \cdot 0.99} = 4.99A$$

It is important to define the following ratios in order to continue describing the energetic relationships in the PFC:

Equation 11

$$k_{min} = \sqrt{2}\frac{VAC_{min}}{V_{out}} \quad k_{min} = \sqrt{2}\frac{90Vac}{400V} = 0.32$$

Equation 12

$$k_{max} = \sqrt{2}\frac{VAC_{max}}{V_{out}} \quad k_{max} = \sqrt{2}\frac{265Vac}{400V} = 0.94$$

From *Equation 11* and *Equation 12*:

Line peak current:

Equation 13

$$I_{PKmax} = \frac{2 \cdot P_{in}}{k_{min} \cdot V_{out}} \quad I_{PKmax} = \frac{2 \cdot 444.44W}{0.32 \cdot 400V} = 6.98A$$

Inductor Ripple-ΔILpk:

Equation 14

$$\Delta IL_{pk} = \frac{6 \cdot k_r}{8 - 3 \cdot k_r} \cdot I_{PK\,max} \quad \Delta IL_{pk} = \frac{6 \cdot 0.34}{8 - 3 \cdot 0.34} \cdot 6.98A = 2.04A$$

Inductor peak current:

Equation 15

$$IL_{pk\,max} = \frac{8}{8 - 3 \cdot k_r} \cdot I_{PK\,max} \quad IL_{pk\,max} = \frac{8}{8 - 3 \cdot 0.34} \cdot 6.98A = 8.01A$$

It is also possible to calculate the RMS current flowing into the switch and into the diode, needed to calculate the losses of these two elements.

RMS switch current:

Equation 16

$$ISW_{rms} = \frac{P_{in}}{k_{min} \cdot V_{out}} \cdot \sqrt{2 - \frac{16 \cdot k_{min}}{3\pi}} \quad ISW_{rms} = \frac{400W}{0.32 \cdot 400V} \cdot \sqrt{2 - \frac{16 \cdot 0.32}{3\pi}} = 4.22A$$

RMS diode current:

Equation 17

$$ID_{rms} = \frac{P_{in}}{k_{min} \cdot V_{out}} \cdot \sqrt{\frac{16k_{min}}{3\pi}} \quad ID_{rms} = \frac{400W}{0.32 \cdot 400V} \cdot \sqrt{\frac{16 \cdot 0.32}{3\pi}} = 2.57A$$

It is worth remembering that the accuracy of the approximate energetic relationships described here is quite good at maximum load for low values of parameter k, that is, at low line voltage, but worsens at high line and as the power throughput is reduced. Since in the design phase current stress is calculated at maximum load and minimum line voltage, their accuracy is acceptable for design purposes.

4.3 Power section design

4.3.1 Bridge rectifier

The input rectifier bridge can use standard slow recovery, low-cost devices.

Typically a 600 V device is selected in order to have good margin against mains surges. An NTC resistor limiting the current at turn-on is required to avoid overstress to the diode bridge.

The rectifier bridge power dissipation can be calculated using *Equation 18*, *Equation 19*, and *Equation 20*. The threshold voltage (V_{th}) and dynamic resistance (Rdiode) of a single diode of the bridge can be found in the component datasheet.

Equation 18

$$\bar{I}_{inrms} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 4.99A}{2} = 3.53A$$

Equation 19

$$\bar{I}_{in_avg} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 4.99A}{\pi} = 2.25A$$

The power dissipated on the bridge is:

Equation 20

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^2_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in_avg}$$

$$P_{bridge} = 4 \cdot 0.025\Omega \cdot (3.53A)^2 + 4 \cdot 0.7V \cdot 2.25A = 7.53W$$

4.3.2 Input capacitor

The input filter capacitor (Cin) is placed across the diode bridge output. This capacitor must smooth the high-frequency ripple and must sustain the maximum instantaneous input voltage. In a typical application an EMI filter is placed between the mains and the PFC circuit. In this application the EMI filter is reinforced by a differential mode Pi-filter after the bridge to reject the differential noise coming from the whole switching circuit. The design of the EMI filter (common mode and differential mode) is not described here. The value of the input filter capacitor can be calculated as follows, simply considering the output power that the PFC should deliver at full load:

Equation 21

$$C_{in} = 2.5 \cdot 10^{-3} \cdot P_{out} \quad C_{in} = 2.5 \cdot 10^{-3} \cdot 400W = 1\mu F$$

The maximum value of this capacitor is limited to avoid line current distortion. The value chosen for this design is 1µF.

4.3.3 Output capacitor

The output bulk capacitor (Co) selection depends on the DC output voltage *(4)*, the allowed maximum voltage *(7)*, and the converter output power *(3)*.

The 100/120 Hz (twice the mains frequency) voltage ripple (ΔVout = peak-to-peak ripple value) *(8)* is a function of the capacitor impedance and the peak capacitor current:

Equation 22

$$\Delta V_{out} = 2 \cdot I_{out} \cdot \sqrt{\frac{1}{(2\pi \cdot 2f_l \cdot C_O)^2} + ESR^2}$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

Equation 23

$$C_O \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_l \cdot V_{out} \cdot \Delta V_{out}} \quad C_O \geq \frac{400W}{2\pi \cdot 47Hz \cdot 400V \cdot 10V} = 338\mu F$$

Vout is usually selected in the range of 1.5% of the output voltage. Although ESR does not usually affect the output ripple, it should be taken into account for power loss calculations. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

Equation 24

$$I_{Crms} = \sqrt{ID^2_{rms} - I^2_{out}} \quad I_{Crms} = \sqrt{(2.56A)^2 - (1.0A)^2} = 2.36A$$

If the PFC stage must guarantee a specified holdup time, the selection criterion of the capacitance changes. Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage ($V_{out\ min}$) that is the minimum output voltage value (which takes load regulation and output ripple into account). $V_{out\ min}$ is the minimum output operating voltage before the 'power fail' detection and consequent stopping by the downstream system supplied by the PFC.

Equation 25

$$C_O = \frac{2 \cdot P_{out} \cdot t_{Hold}}{(V_{out} - \Delta V_{out})^2 - V^2_{out\,min}} \quad C_O = \frac{2 \cdot 400W \cdot 20ms}{(400V - 10V)^2 - (300V)^2} = 242.3\mu F$$

A 20% tolerance on the electrolytic capacitors must be taken into account for the right dimensioning.

Following the relationship (*Equation 25*), for this application a capacitor Co = 330 µF (450 V) has been selected in order to maintain a holdup capability for 22 ms. The actual output voltage ripple with this capacitor is also calculated. In detail:

Equation 26

$$t_{hold} = \frac{C_O \cdot \left[\left(V_{out} - \Delta V_{out} \right)^2 - V_{outmin}^2 \right]}{2 \cdot P_{out}} \quad t_{hold} = \frac{330\mu F \cdot \left[(400V - 10V)^2 - (300V)^2 \right]}{2 \cdot 400W} = 22ms$$

As expected, the ripple variation on the output is:

Equation 27

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_O} \quad \Delta V_{out} = \frac{1.0A}{2 \cdot \pi \cdot 47Hz \cdot 330\mu F} = 10.2V$$

4.3.4 Boost inductor

In the continuous mode approach, the acceptable current ripple factor, Kr, can be considered as between 10% to 35%. For this design, the maximum specified current ripple factor is 34%.

To calculate the required inductance L of the boost inductor, use the following formula with a 3.76 µs off-time set at 90 VAC (see the following ZCD pin dimensioning for finding the correct value):

Equation 28

$$L(VAC) = (1 - k_{min}) \cdot \frac{V_{out}}{\Delta IL_{pk}} T_{OFF}(VAC) \quad L(VAC_{min}) = (1 - 0.32) \cdot \frac{400V}{2.04A} 3.76\mu s = 501\mu H$$

After calculating the inductor value at low mains and at high mains $L(VAC_{max})$, $L(VAC_{min})$ (*Equation 28*) depending also on the off-time, the minimum value must be taken into account. It becomes the maximum inductance value for the PFC dimensioning.

Figure 8 shows the switching frequency versus the θ angle calculated inverting *Equation 28* with a 500 µH boost inductance and fixing the line voltage at minimum and maximum values.

Figure 8. Switching frequency fixing the line voltage

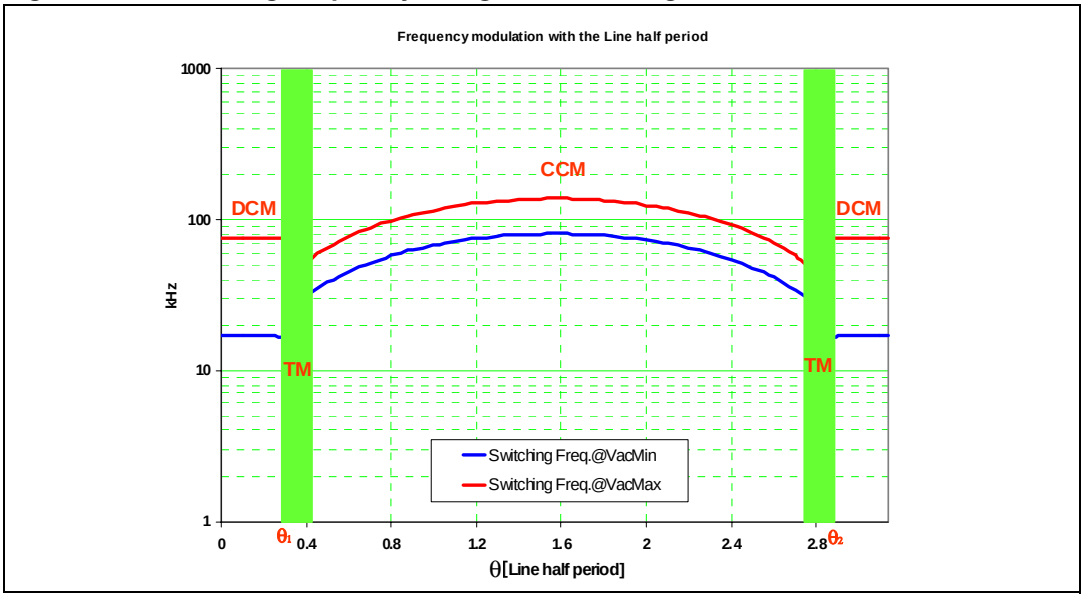
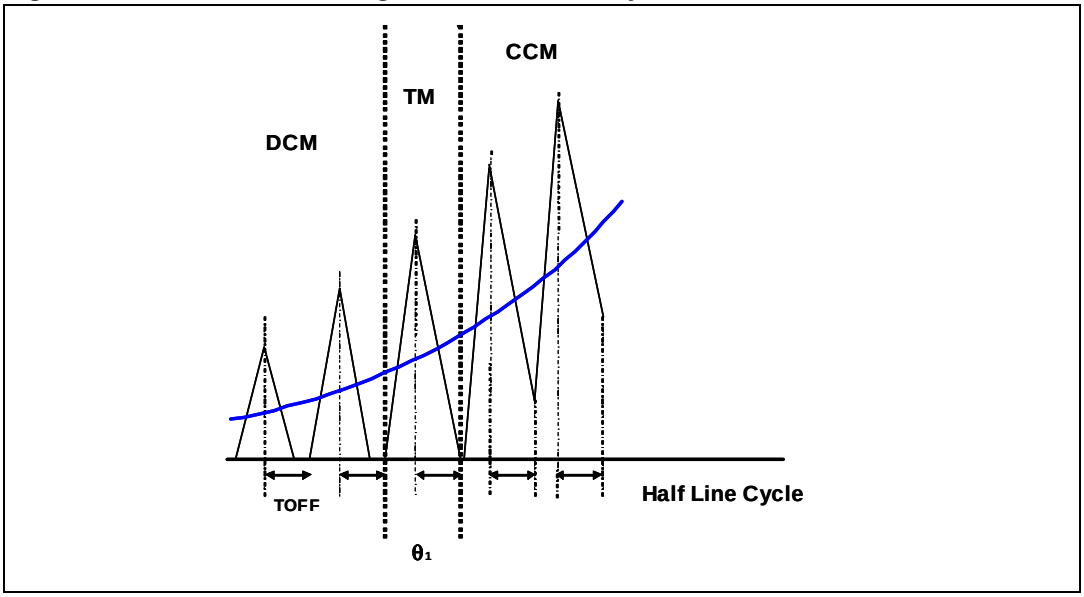


Figure 9. The effect of fixing off-time - boundary between DCM and CCM



The effect of fixing the off-time is generating a continuous conduction mode in the center region of the line half-cycle between the two transition angles. Close to the zero-crossing, the system works in discontinuous conduction mode and in transition mode at the boundary.

The inductor core size is determined assuming a peak flux density Bx ~0.25 T (depending on the ferrite grade selected and relevant specific losses) and calculating the maximum current according to *Equation 15* as a function of the maximum current sense pin clamping voltage and sense resistor value.

DC and AC copper losses and ferrite losses must also be calculated to determine the maximum temperature rise of the inductor.

4.3.5 Power MOSFET selection and power dissipation calculation

The selection of the MOSFET concerns mainly its $R_{DS(on)}$, basically proportional to the output power. The MOSFET breakdown voltage is selected considering the PFC nominal output voltage *(4)* and adding some margin (20%) to guarantee reliable operation.

Therefore, a voltage rating of 500 V (1.2 · Vout = 480 V) is selected. Using its current rating as a rule of thumb, we can select a device having ~ 3 times the RMS switch current (*Equation 16*) but, the power dissipation calculation gives the final confirmation that the selected device is the right one for the circuit, also taking into account the heat sink dimensions. For example in a 400 W PFC application two parallel STP12NM50FP MOSFETs can be selected.

The MOSFET's power dissipation depends on conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

Equation 29

$$P_{cond}(VAC) = RDS_{on} \cdot (ISW_{rms}(VAC))^2$$

Because normally in the datasheets the $R_{DS(on)}$ is given at ambient temperature (25°C) to calculate correctly the conduction losses at 100°C (typical MOSFET junction operating temperature), a factor of 1.75 to 2 should be taken into account. The exact factor can be found on the device datasheet.

Now, combining *Equation 29* and *Equation 16*, the conduction losses referred to a 1 Ω $R_{DS(on)}$, at ambient temperature as a function of Pin and VAC can be calculated:

Equation 30

$$P'_{cond}(VAC) = 2 \cdot (ISW_{rms}(VAC))^2 = 2 \cdot \left(\frac{P_{in}}{k(VAC) \cdot V_{out}} \cdot \sqrt{2 - \frac{16 \cdot k(VAC)}{3\pi}} \right)^2$$

The switching losses due to the MOSFET current-voltage I_{MOS}, V_{MOS} crossing occurs at turn-on and turn-off because of the FOT operation and can be basically expressed by:

Equation 31

$$P_{switch}(VAC) = V_{MOS} \cdot I_{MOS} \cdot \left(\frac{t_{rise} + t_{fall}}{2} \right) \cdot f_{sw}(VAC)$$

Because the switching frequency depends on the input line voltage and on the position on the sinusoidal waveform, it can be demonstrated that from *Equation 31* the switching losses per 1 µs of current rise and fall time can be written as:

Equation 32

$$P'_{switch}(VAC) = V_{out} \cdot \left(IL_{pk\,max} - \frac{\Delta IL_{pk}}{2} \right) \cdot \frac{1}{\pi} \int_0^{\pi} (\sin\vartheta)^2 \cdot f_{sw}(VAC, \theta) \cdot d\vartheta$$

From the STP12NM50FP datasheet $t_{rise} = t_{fall} = 0.01$ µs is the crossover time at turn-on and off. At turn-on the losses are due to the discharge of the total drain capacitance inside the MOSFET itself. In general, the capacitive losses are given by:

Equation 33

$$P_{cap}(VAC) = \frac{1}{2} \cdot C_d \cdot V^2_{MOS} \cdot f_{sw}(VAC)$$

Where C_d is the total drain capacitance including the MOSFET and the other parasitic capacitances such as inductor etc. At the drain node, V_{MOS} is the drain voltage at MOSFET turn-on.

Taking into account the frequency variation with the input line voltage and the phase angle similar to *Equation 32*, a detailed description of the capacitive losses per 1 nF of total drain capacitance can be calculated as:

Equation 34

$$P'_{cap}(VAC) = \frac{1}{2} \cdot \frac{1}{\pi} \int_0^{\pi} (V_{out})^2 f_{sw}(VAC, \vartheta)\, d\vartheta$$

The total drain capacitance of the two MOSFETs is //C_d = 0.36 nF, Vout is the drain voltage at MOSFET turn-on.

The function of the total losses of the input mains voltage is the sum of the three previous losses from *Equation 30*, *Equation 32*, and *Equation 34*, multiplied for the two parallel MOSFET parameters:

Equation 35

$$P_{loss}(VAC) = RDS_{on} \cdot P'_{cond}(VAC) + \left(\frac{t_{rise} + t_{fall}}{2} \right) \cdot P'_{sw}(VAC) + C_d \cdot P'_{cap}(VAC)$$

From *Equation 35*, using the data relevant to the MOSFET selected and calculating the losses at VAC_{min} and VAC_{max}, we observe that the maximum total losses occurs at VAC_{min} which is 9 W. From this number and the maximum ambient temperature *(13)*, the total maximum thermal resistance required to keep the junction temperature below 125°C is:

Equation 36

$$R_{th} = \frac{125°C - T_{ambx}}{P_{loss}(VAC)} \quad R_{th} = \frac{125°C - 50°C}{9W} = 8.1 \frac{°C}{W}$$

If the result of *Equation 36* is lower than the junction-ambient thermal resistance given in the MOSFET datasheet for the selected device package, a heat sink must be used.

Figure 10. Conduction losses and total losses in the STP12NM50FP MOSFET couples for the 400W FOT PFC

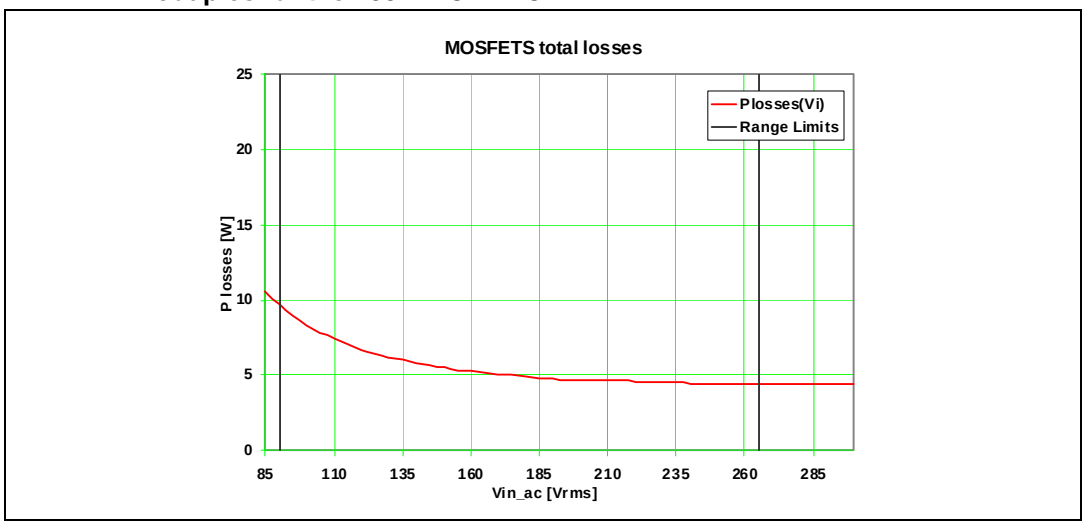


Figure 10 shows the trend of the total losses (*Equation 35*) on the line voltage for the two selected STP12NM50 MOSFETs.

4.3.6 Boost diode selection

Following a similar criterion as that for the MOSFET, the output rectifier can also be selected. A minimum breakdown voltage of 1.2·Vout *(4)* and a current rating higher than 3·Iout (*Equation 8*) can be chosen for a rough initial selection of the rectifier. The correct choice is then confirmed by the thermal calculation. If the diode junction temperature works within 125°C the device has been selected correctly, otherwise a bigger device must be selected. The switching losses can be significantly reduced if an ultra-fast diode is employed. Since this circuit operates in the continuous current mode, the MOSFET must recover the boost diode minority carrier charge at turn-on. Thus, a diode with a small reverse recovery time (trr) must be used.

In this 400 W application an STTH8R06, (600 V, 8 A) has been selected. The STTH8R06 offers the best solution for the continuous current mode operation due to its very fast reverse recovery time, 25 ns typical. This part has a breakdown voltage rating (Vrrm) of 600 V, average forward current rating (Ifave) of 8 A and reverse recovery time (trr) of 25 ns. The rectifier AVG (*Equation 8*) and RMS (*Equation 17*) current values and the parameter V_{th} (rectifier threshold voltage) and Rd (dynamic resistance) given in the datasheet allow the calculation of the rectifier losses.

From the STTH8R06 datasheet, V_{th} is 1.16 V, Rd is 0.08, neglecting the recovery losses:

Equation 37

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2_{rms} \quad P_{diode} = 1.16V \cdot 1.0A + 0.08\Omega \cdot (2.56A)^2 = 1.69W$$

From *(13)* and *Equation 37* the maximum thermal resistance to keep the junction temperature below 125°C is then:

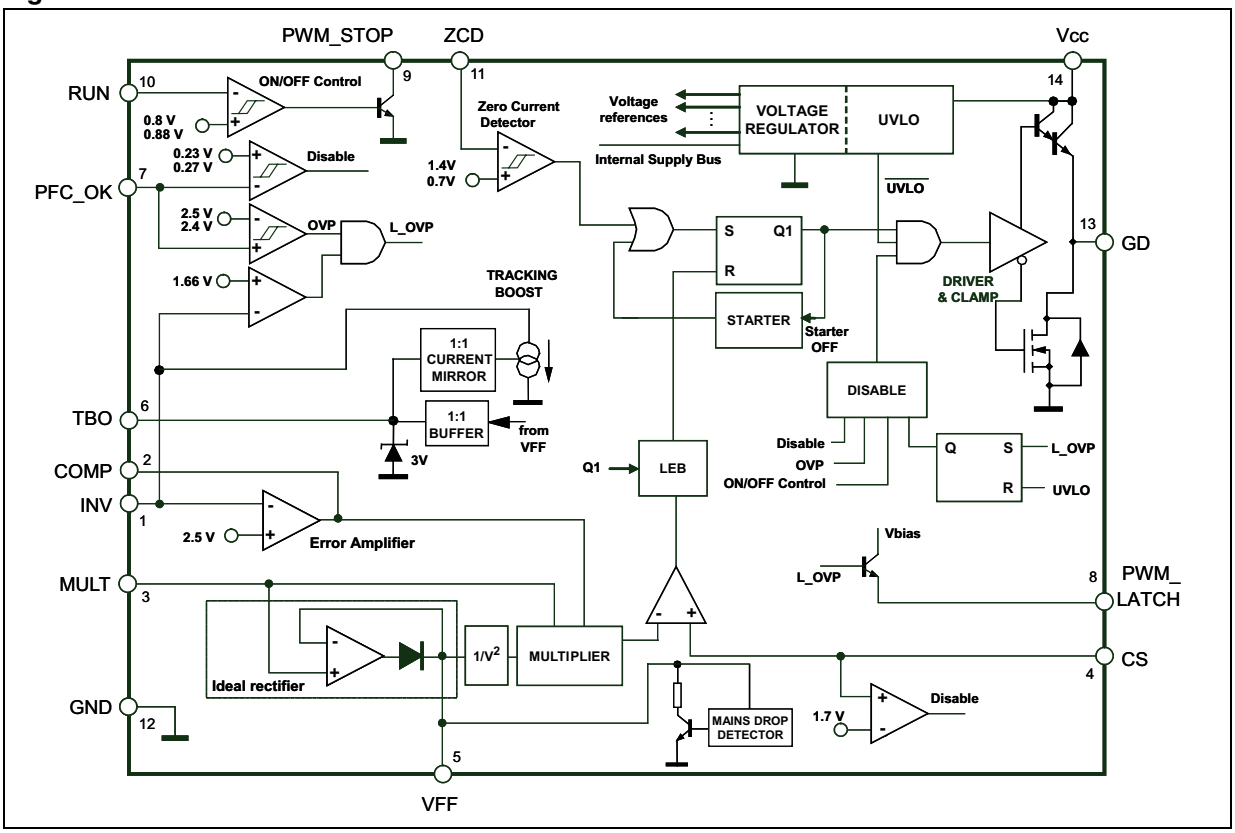
Equation 38

$$R_{th} = \frac{125°C - T_{ambx}}{P_{diode}} \quad R_{th} = \frac{125°C - 50°C}{1.69W} = 44.45\frac{°C}{W}$$

4.3.7 L6563S biasing circuitry

Following the dimensioning of the power components, the biasing circuitry for the L6563S is also described here. For reference, the internal schematic of the L6563S is represented below in *Figure 11*. For more detail on the internal functions please refer to the datasheet.

Figure 11. L6563S internal schematic



Pin 1 (INV): This pin is connected both to the inverting input of the E/A and to the OVP circuitry. A resistive divider is connected between the boost regulated output voltage and this pin. The internal reference on the non-inverting input of the E/A is 2.5 V (typ.), the output voltage (Vout) of the PFC pre-regulator is set at its nominal value, by the resistors ratio of the feedback output divider. R_{outH} and R_{outL} are then selected considering the desired nominal output voltage and the desired output power dissipated on the output divider. For example for a 50 mW output divider dissipation:

Equation 39

$$R_{outH} = \frac{(V_{OUT} - 2.5V)^2}{50mW} \quad R_{outH} = \frac{(400V - 2.5V)^2}{50mW} = 3.160M\Omega$$

With the commercial value selected $R_{outH} = 3M\Omega$

Equation 40

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5V} - 1 \quad \frac{R_{outH}}{R_{outL}} = \frac{400V}{2.5V} - 1 = 159$$

Equation 41

$$R_{outL} = \frac{R_{outH}}{159} \quad R_{outL} = \frac{3M\Omega}{159} = 18.8k\Omega$$

R_{outL} = 62 kΩ in parallel to a 27 kΩ can be selected. Please note that for R_{outH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series have to be used.

Pin 7 (PFC_OK - feedback failure protection) The PFC_OK pin has been dedicated to monitor the output voltage with a separate resistor divider. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (Vovp), usually larger than the maximum Vout that can be expected, including also worst-case load/line transients. For a maximum output voltage Vout max of 430 V and imaging a 50 µA current flowing into the divider:

Equation 42

$$R_L = \frac{V_{REF_PFC_OK}}{I_{divider}} \quad R_L = \frac{2.5V}{50\mu A} = 50k\Omega$$

By selecting a commercial value of 51kΩ

Equation 43

$$R_H = R_L \cdot \left(\frac{V_{OUT_MAX}}{V_{REF_PFC_OK}} - 1 \right) \quad R_H = 51k\Omega \cdot \left(\frac{430V}{2.5V} - 1 \right) = 8.721M\Omega$$

Connecting in series two 3.3 MΩ resistors and one 2.2 MΩ resistor a total value of 8.8 MΩ can be obtained.

Notice that both feedback dividers connected to the L6563S pin #1 (INV) and pin #7 (PFC_OK) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above can handle “normal” over-voltage conditions, that is, those resulting from an abrupt load/line change or occurring at start-up. If the over-voltage is generated by a feedback disconnection for instance, when one of the upper resistors of the output divider fails to open, an additional circuitry detects the voltage drop of pin INV. If the voltage on pin INV is lower than 1.66V (Typ.) and at same time the OVP is active, a feedback failure is assumed.

Therefore, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced to below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of the L6563S goes below 6 V and that one of the PWM controllers goes below its UVLO threshold. Note that this function offers complete protection not only against feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating results in shutting down the IC and stopping the preregulator. Moreover, the PFC_OK pin doubles its function as a not-latched IC disable: a voltage below 0.23 V shuts down the IC, reducing its consumption to below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

Pin 2 (COMP): This pin is the output of the E/A that is fed into one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and INV (pin#1). It must be designed with a narrow bandwidth in order to avoid the system rejecting the output voltage ripple (100 Hz) that would bring high distortion of the input current waveform. A theoretical criterion to define the compensation network value is to set the E/A bandwidth (BW) from 20 to 30 Hz.

For a more complex way of compensating the FOT PFC please refer to [1], [2], [3].

A compensated two-pole feedback network for this 400 W FOT PFC is obtained with the following values:

$$C_{compP} = 100nF \quad C_{compS} = 1\mu F \quad R_{compS} = 56k\Omega \tag{14}$$

to which the following open-loop transfer function and its phase function correspond.

Figure 12. Open-loop transfer function-bode plot

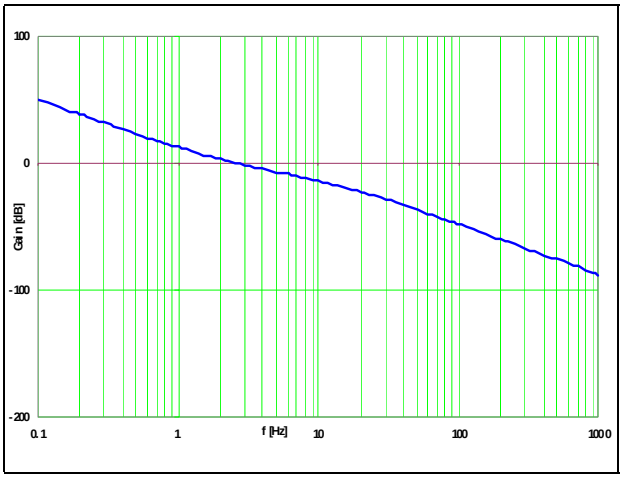
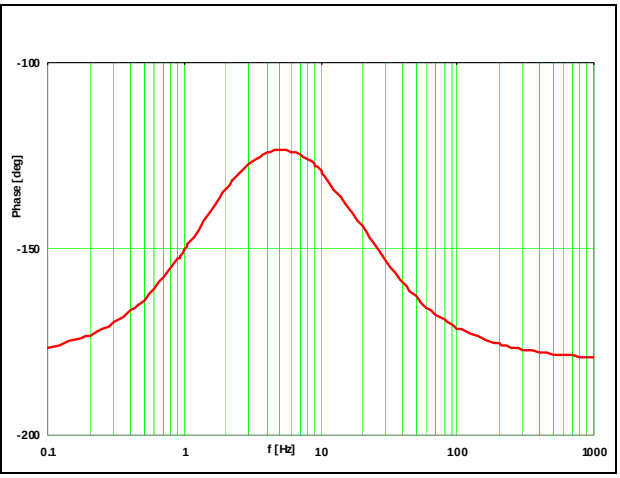


Figure 13. Phase



The two bode plot charts are in reference to the PFC operating at the main voltage set point of 265 VAC and full load. In this condition the crossover frequency is fc = 4 Hz, the phase margin is 50° and the third harmonic distortion is under 3%.

Pin 4 (CS): Pin #4 is the inverting input of the current sense comparator. Through this pin, the L6563S reads the instantaneous inductor current, converted in a proportional voltage by an external sense resistor (Rs). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in OFF-state until the PWM latch is set again by the ZCD signal. The pin is equipped with 150 ns leading-edge blanking for improved noise immunity.

The sense resistor value (Rs) can be calculated as follows. For the 400 W PFC it is:

Equation 44

$$R_s < \frac{Vcs_{min}}{IL_{pk\,max}} \quad R_s < \frac{1.0V}{8.01A} = 0.124\Omega$$

Where:

- IL_{pk}: it is the maximum peak current in the inductor, calculated as described in 4.2
- Vcs_{min} = 1.0 V, it is the minimum voltage admitted on the L6563S current sense (on the datasheet).

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current is calculated considering the maximum voltage Vcs_{max} admitted on the L6563S (on the datasheet):

Equation 45

$$IL_{pksat} = \frac{Vcs_{max}}{R_s} \quad IL_{pksat} = \frac{1.16V}{0.12\Omega} = 9.67A$$

The calculated ILpkx is the value at which the boost inductor must not be in saturation and it is used for calculating the inductor number of turns and air gap length.

The power dissipated by Rs is given by:

Equation 46

$$P_s = R_s \cdot ISW_{rms}^2 \quad P_s = 0.12\Omega \cdot (4.22)^2 = 2.14W$$

According to the result, for example four parallel resistors of 0.47 Ω with 1 W of power rating can be selected.

Pin 3 (MULT): The MULT pin is the second multiplier input. It is connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

Equation 47

$$V_{CS} = V_{CS_OFFSET} + k_m \cdot \frac{(V_{COMP} - 2.5V) \cdot V_{MULT}}{V_{FF}^2}$$

Where:

- V_{CS} (Multiplier output) is the reference for the current sense (V_{CS_OFFSET} is its offset).
- k = 0.45 (Typ.) is the multiplier gain.
- V_{COMP} is the voltage on pin 2 (E/A output).
- V_{MULT} is the voltage on pin 3. V_{FF} is the second input to the multiplier for $1/V^2$ function. It compensates the control loop gain dependence on the mains voltage. The voltage at this pin is a DC level equal to the peak voltage on the MULT pin (#3).

Figure 14. Multiplier characteristics family for V_{FF} =1 V

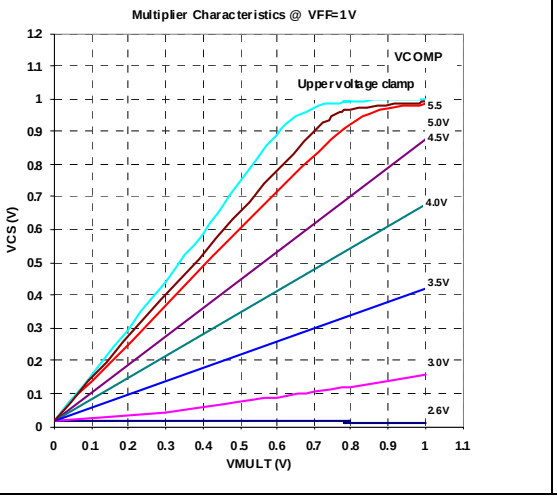
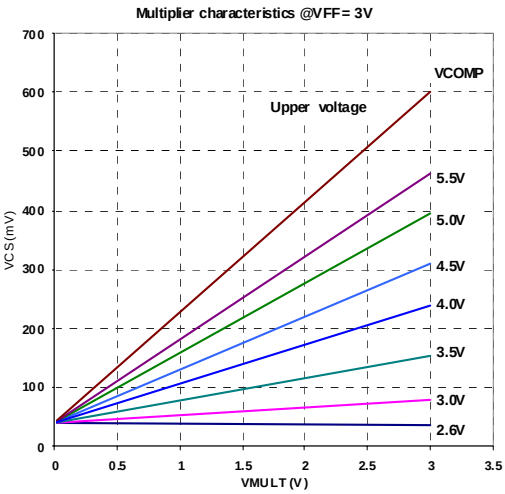


Figure 15. Multiplier characteristics family for V_{FF}=3 V



A complete description is given by the diagram in *Figure 14* and *15* which shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed within the range 0 to 3 V of V_{MULT} and the range 0 to 1.16 V (typ.) of Vcs, while the minimum guaranteed value of the maximum slope of the characteristics family (typ.) is:

Equation 48

$$\frac{dV_{CS}}{dV_{MULT}} = 1.66\frac{V}{V}$$

The voltage on the MULT pin is used also to derive the information on the RMS mains voltage for the V_{FF} compensation.

The suggested procedure to properly set the operating point of the multiplier is now described. First, the maximum peak value for V_{MULT}, $V_{MULTmax}$ is selected. This value, which occurs at maximum mains voltage, should be 3 V or thereabouts in wide range mains and less in the case of single mains. The sense resistor selected is Rs = 0.12 Ω and it is described in the pin #4 section. According to the L6563S datasheet and to the linearity setting of the pin, the maximum voltage accepted on the multiplier input is:

$$VMULT_{max} = 3V \quad (15)$$

Where ILpk and Rs have been already calculated, 1.66 is the Multiplier maximum slope, reported on the datasheet.

From *15* the maximum required divider ratio is calculated as:

Equation 49

$$k_p = \frac{V_{MULTmax}}{\sqrt{2}\cdot VAC_{max}} = \frac{3.00V}{\sqrt{2}\cdot 265Vac} = 8\cdot 10^{-3},$$

Supposing there is a 60 µA current flowing into the multiplier divider the lower resistor value can be calculated as:

Equation 50

$$R_{multL} = \frac{V_{MULTmax}}{60\mu A} = \frac{3.00V}{60\mu A} = 50k\Omega$$

A commercial value of 51 kΩ for the lower resistor is selected. The upper resistor value can now be calculated:

Equation 51

$$R_{multH} = \frac{1-k_p}{k_p} R_{multL} = \frac{1-8\cdot10^{-3}}{8\cdot10^{-3}} 51k\Omega = 6.319M\Omega$$

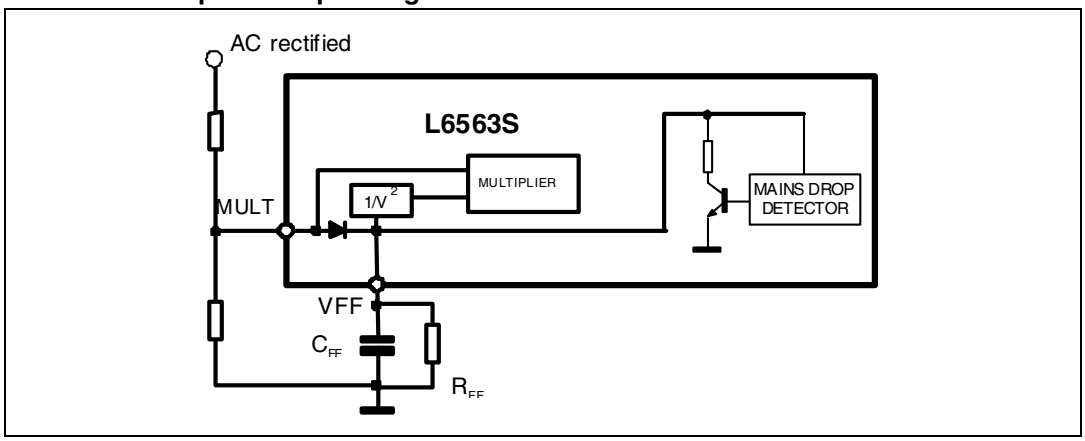
In this application example a RmultH = 6.6 MΩ and a RmultL = 51 kΩ have been selected. Please note that for RmultH a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series have to be used.

The voltage on the multiplier pin with the selected component values re-calculated at minimum line voltage is 1.1 V and at maximum line voltage is 2.99 V. Therefore the multiplier works correctly within its linear region.

Pin 5 (voltage feed forward): The power stage gain of PFC preregulators varies with the square of the RMS input voltage. So does the crossover frequency f_c of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get f_c = 20 Hz @ 264 VAC means having f_c 4 Hz @ 88 VAC, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage. Voltage feedforward can compensate for the gain variation with the line voltage and allow the overcoming of all the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (*Figure 16*). In this way a change of the line voltage causes an inversely proportional change of the half-sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier, output is halved and vice versa) so that the current reference is adapted to the new operating conditions with, ideally, no need to invoke the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves dynamic behavior significantly at low line and simplifies loop design. In fact, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off is required. The device realizes

voltage feedforward with a technique that makes use of just two external parts and that limits the feedforward time constant trade-off issue to only one direction.

Figure 16. Mains detector and discharge resistor allow fast response to sudden line drops not depending on the external RC



A capacitor C_{FF} and a resistor R_{FF}, both connected from the V_{FF} (pin 5) pin to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (pin 3). In a case where the V_{FF} pin is connected directly to the RUN pin as in *Figure 17*, the following value can be selected:

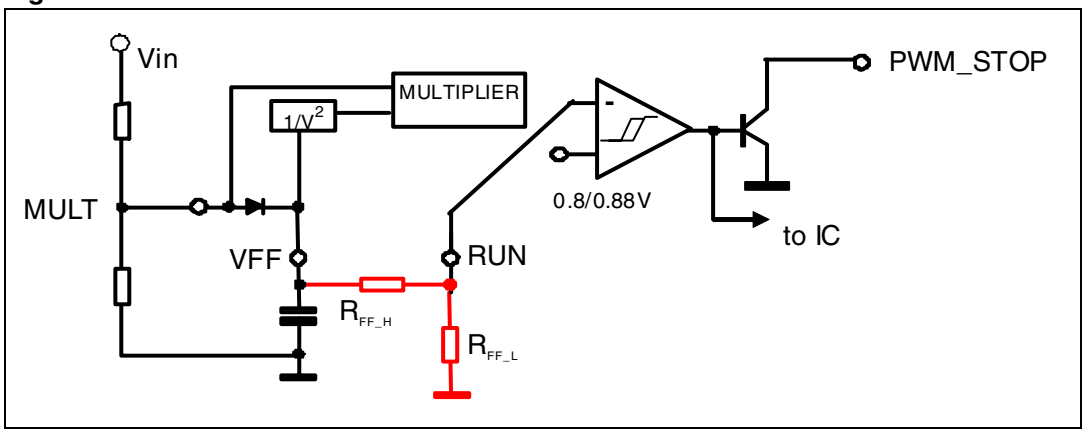
$$C_{FF} = 1\mu F \quad R_{FF} = 1M\Omega \tag{16}$$

R_{FF} provides a means to discharge C_{FF} when the line voltage decreases (see *Figure 16*). In this way, in the case of a sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode and no appreciable overshoot is visible at the preregulator's output; in the case of line voltage drop, C_{FF} is discharged with the time constant $R_{FF} \cdot C_{FF}$, which can be in the hundred ms to achieve an acceptably low steady-state ripple and have low current distortion; consequently the output voltage can experience a considerable undershoot, like in systems with no feedforward compensation.

Pin 10 (RUN): Remote ON/OFF control. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.88 V.

The Brownout function can be easily implemented by connecting to the RUN pin through a divider to the V_{FF} pin as shown in *Figure 17*.

Figure 17. Brownout function in L6563S and L6563H



The divider replaces the discharge resistor R_{FF} shown in *Figure 16*. It should be selected in order to have a similar time constant of *(16)* but also to obtain the PFC startup at minimum input mains voltage VACmin, (in this design 90 VAC), as specified in (1).

Therefore, we can set:

$$C_{FF} = 1\mu F \qquad (17)$$

Referring to *Figure 17* and considering the peak of the minimum input mains voltage $\sqrt{2} \cdot 90Vac$, the corresponding voltage on the V_{FF} pin is:

Equation 52

$$V_{FF@V_{START}} = \sqrt{2} \cdot V_{START} \cdot \frac{R_{multL}}{R_{multL} + R_{multH}} - \Delta V$$

$$V_{FF@V_{START}} = \sqrt{2} \cdot 90Vac \cdot \frac{51k\Omega}{51k\Omega + 6.6M\Omega} - 20mV = 0.973V$$

ΔV is the voltage drop between the V_{FF} and MULT pins.

Now, considering the RUN pin enable threshold (0.88 V is the typical value given on the datasheet), the RUN pin divider ratio can be calculated as follow:

Equation 53

$$\frac{V_{RUN_EN}}{V_{FF@V_{START}}} = \frac{R_{FF_L}}{R_{FF_L} + R_{FF_H}} = 0.904$$

Setting up RFF_L = 1MΩ, RFF_H can be calculated from *Equation 53*:

Equation 54

$$R_{FF_H} = \left(\frac{V_{FF@V_{START}}}{V_{RUN_EN}} - 1 \right) \cdot R_{FF_L} \qquad R_{FF_H} = \left(\frac{0.973V}{0.88V} - 1 \right) \cdot 1M\Omega = 105k\Omega$$

The result of the previous formula (*Equation 54*) is based on typical values and doesn't take into account the V_{RUN_EN} threshold and the resistor tolerances. In order to have the startup

at minimum mains voltage, as set in *Equation 1*, guarantee against parameter variation, the mentioned tolerances should be taken into account, making some calculations considering the worst cases.

In this case, taking into account the resistors and threshold tolerances, 1 MΩ and a 56 kΩ have been calculated, therefore the actual divider ratio is 0.946. Then the following check can be done:

Equation 55

$$V_{FF_ENABLE} = V_{RUN_EN} \cdot \frac{R_{FF_L} + R_{FF_H}}{R_{FF_L}} \quad V_{FF_ENABLE} = 0.88V \cdot \frac{1M\Omega + 56k\Omega}{1M\Omega} = 0.923V$$

Equation 56

$$V_{in_START} = \left(\frac{V_{FF_EN} + 20mV}{\sqrt{2}} \right) \cdot \frac{R_{multH} + R_{multL}}{R_{multL}}$$

$$V_{in_START} = \left(\frac{0.923V + 20mV}{\sqrt{2}} \right) \cdot \frac{6.6M\Omega + 51k\Omega}{51k\Omega} = 87Vac$$

Equation 57

$$V_{FF_DISABLE} = V_{RUN_DIS} \cdot \frac{R_{FF_L} + R_{FF_H}}{R_{FF_L}} \quad V_{FF_DISABLE} = 0.80V \cdot \frac{1M\Omega + 56k\Omega}{1M\Omega} = 0.844V$$

Equation 58

$$V_{in_STOP} = \left(\frac{V_{FF_DIS} + 20mV}{\sqrt{2}} \right) \cdot \frac{R_{multH} + R_{multL}}{R_{multL}}$$

$$V_{in_STOP} = \left(\frac{0.844V + 20mV}{\sqrt{2}} \right) \cdot \frac{6.6M\Omega + 51k\Omega}{51k\Omega} = 79.9Vac$$

Pin 11 (ZCD) is the input of the zero current detector circuit. In FOT mode, it is connected to the Line-Modulated-Fixed-Off-Time circuit seen in *Figure 6*. Taking into account the information contained in *Section 3*, the starting point for the design of that circuit is the pair of the desired values for T_{OFF} on the top of the line voltage sinusoid at minimum (T_{OFF} @ V_{ACmin}) and maximum line (T_{OFF} @ V_{ACmax}) obtained by setting the switching frequency on the peak of the sinusoid at low mains and considering the minimum on-time of the L6563S:

Equation 59

$$T_{OFF}(VAC_{min}) = \frac{k_{min}}{f_{sw\,min}} \quad T_{OFF}(VAC_{min}) = \frac{0.32}{80kHz} - 220ns = 3.76\mu s$$

Equation 60

$$T_{OFF}(VAC_{max}) = \frac{T_{ONmin} \cdot k_{max}}{1 - k_{max}} \quad T_{OFF}(VAC_{max}) = \frac{450ns \cdot 0.94}{1 - 0.94} - 220ns = 6.1\mu s$$

Where f_{swmin} is the switching frequency on the top of the sinusoid of the input voltage at V_{ACmin} = 90 VAC (*Figure 18*) and 220 ns is a corrector factor in order to consider the delay between the ZCD and GD signal.

Considering the ratio between *Equation 60*, *Equation 59*:

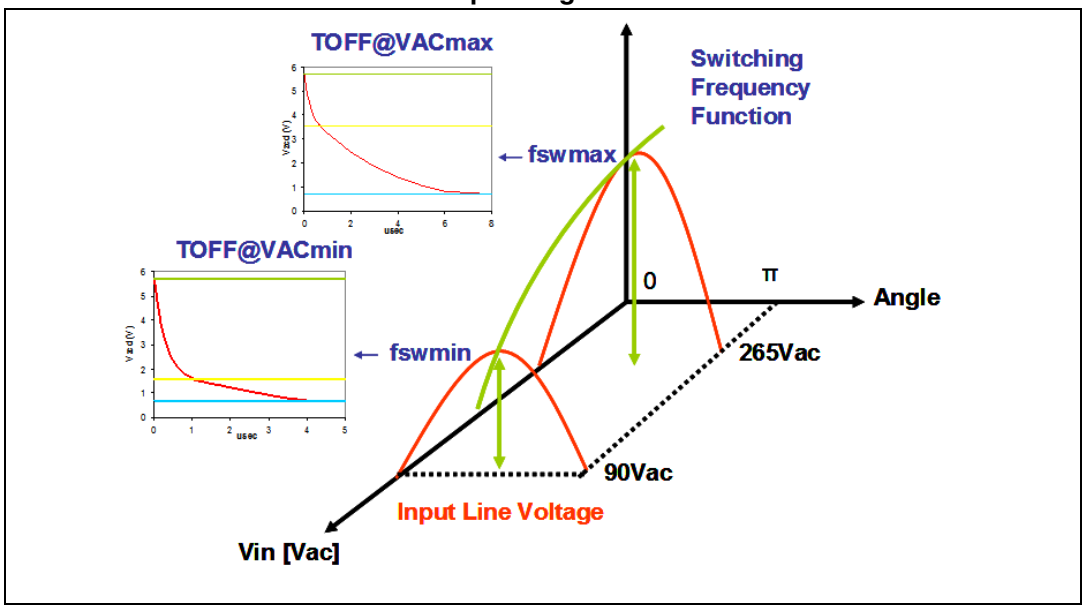
Equation 61

$$\rho_x = \frac{T_{OFF}(VAC_{max})}{T_{OFF}(VAC_{min})} \quad \rho_x = \frac{6.1\mu s}{3.76\mu s} = 1.63$$

In the formula *Equation 59*, *Equation 60*, the delay between the ZCD signal and the gate drive signal is taken into account in order to increase the accuracy of the mathematical model.

From the theory of the line modulation fixed off-time, T_{OFF} is increasing with the line voltage so that at maximum line voltage the condition T_{ON}>T_{ONmin} is always true [*4*]. This is important in order to avoid line distortion [*5*].

Figure 18. Switching frequency function on the peak of the sinusoid input voltage waveform and the corresponding off-time value



Now considering the two discharging resistors R and R0 of the circuit in *Figure 6*, the ratio is defined:

Equation 62

$$K_1 = \frac{R}{R_0 + R}$$

where 0 < K1 < 1. Through the definition of the k2 parameter the expected time constant τ=(R//R0)C is underlined, this is necessary to achieve the desired T_{OFF}@90 VAC.

Equation 63

$$K_2 = \frac{T_{OFF}(VAC_{min})}{\tau}$$

Finding a way to obtain K1 and K2 means to gain the values of R and R0 and the discharging time constant of the C capacitor.

The following part describes the mathematical way to obtain the two parameters K1 and K2. Combining *Equation 61*, *Equation 62*, *Equation 63* with the expression of the off-time (*Equation 5*) the following expressions are obtained:

Equation 64

$$\rho(V_{multmin},k_1) = \frac{\left[\ln\left[\frac{\left[V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F\right]\cdot(1-k_1)}{\left[V_{ZCDclamp}-\left[V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F\right]\right]\cdot(k_1)}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}\cdot\frac{VAC_{max}}{VAC_{min}}+V_F}\right)\right]}{\left[\ln\left[\frac{[V_{multmin}+V_F]\cdot(1-k_1)}{[V_{ZCDclamp}-[V_{multmin}+V_F]]\cdot(k_1)}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}+V_F}\right)\right]}$$

Equation 65

$$k_2(V_{multmin},k_1) = \left[\frac{-1}{1-k_1}\cdot\ln\left[\frac{[V_{multmin}+V_F]\cdot(1-k_1)}{V_{ZCDclamp}-[V_{multmin}+V_F]\cdot k_1}\right]^{1-k_1}+\ln\left(\frac{V_{ZCDtrigger}}{V_{multmin}+V_F}\right)\right]$$

From *Equation 61* and *Equation 64*, solving the following equation:

Equation 66

$$\rho(V_{multmin},k_1) - \rho_x = 0 \quad K_1 = 0.903$$

And then substituting the K1 value into the *Equation 65* expression, the k2 parameter is obtained:

Equation 67

$$K_2 = k_2(V_{multmin},k_1) \quad K_2 = 11.17$$

From the values of K1 and K2 it is possible to calculate the time constant τ=(R1//R2) C necessary to achieve the desired T_{OFF}@90 VAC:

Equation 68

$$\tau = \frac{T_{OFF}(VAC_{min})}{K_2} \quad \tau = \frac{3.76\mu s}{11.17} = 336.35ns$$

Now, by selecting a capacitor C in the hundred picofarad range or a few nanofarads, for example a C = 220 pF, it is possible to determine the required equivalent resistance value:

Equation 69

$$R_{eq} = \frac{\tau}{C} \quad R_{eq} = \frac{336.35ns}{220pF} = 1.53k\Omega$$

From *Equation 62*, R and R0 are found:

Equation 70

$$R = \frac{R_{eq}}{1-K_1} \quad R = \frac{1.53k\Omega}{1-0.903} = 15.79k\Omega$$

Equation 71

$$R_0 = \frac{R_{eq}}{K_1} \quad R_0 = \frac{1.53k\Omega}{0.903} = 1.5k\Omega$$

A commercial value R = 15 kΩ and an R0 = 1.5 kΩ has been chosen.

Figure 19 and *Figure 20* show the trend of the off-time and the switching frequency vs the input mains voltage. The PFC inner current loop is working in the range 80 kHz-150 kHz.

Due to the tolerance of the capacitor selected C and the two discharging resistors, it is important to take into account a variation on the switching frequency in a real board of about ± 10%.

Figure 19. Off-time vs. input mains voltage

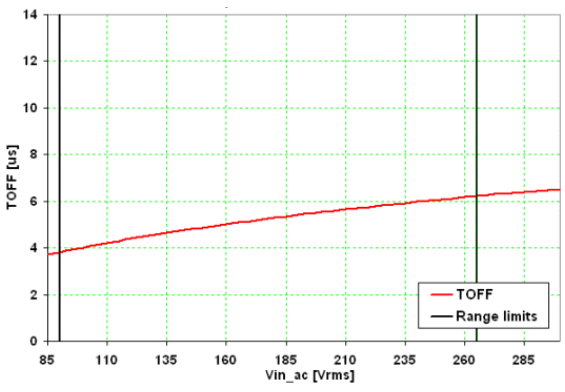
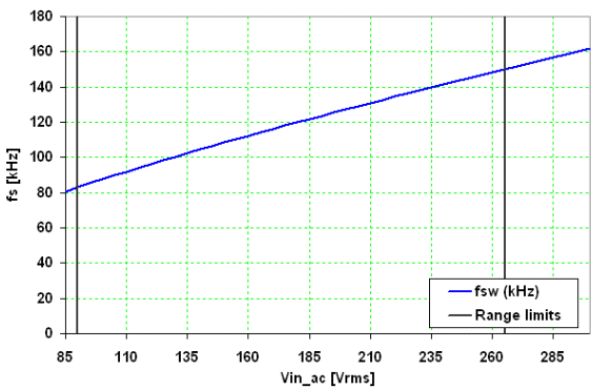


Figure 20. Switching frequency vs. input mains voltage



Finally limiting resistor Rs should be selected according to the inequalities in *Equation 6*:

Equation 72

$$\frac{15V - 5.7V - 0.6V}{10mA + \frac{5.7V}{1.53k\Omega}} < Rs < 1.53k\Omega \cdot \frac{10V - 5.7V - 0.6V}{5.7V}$$

and the Speed-Up capacitor Cs using *Equation 7*:

Equation 73

$$Cs < 220pF \cdot \frac{5.7V}{15V - 5.7V - 0.6V}$$

That means that after calculation:

Equation 74

$$726\Omega < Rs < 1k\Omega$$

Equation 75

$$Cs < 144pF$$

For example, a commercial value of the limiting resistor of 1 kΩ and a speed-up capacitor of 100 pF can be selected for this application.

Pin 6 (TBO): In some applications it may be advantageous to regulate the output voltage of the PFC preregulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost preregulators. This is commonly referred to as the “tracking boost” or “follower boost” approach.

With this IC the function can be realized by connecting a resistor (RT) between the TBO pin and ground. The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is then representative of the mains RMS voltage. The resistor defines a current, equal to V(TBO)/RT, that is internally 1:1 mirrored and sunk from the INV pin (pin 1) input of the error amplifier. In this way, when the mains voltage increases, the voltage at the TBO pin also increases and therefore so does the current flowing through the resistor connected between the TBO and GND. Then a larger current is sunk by the INV pin and the output voltage of the PFC preregulator is forced to get higher. Obviously, the output voltage moves in the opposite direction if the input voltage decreases. To avoid undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3 V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open: the device regulates a fixed output voltage.

Pin 8 (PWM_LATCH): Output pin for fault signaling. During normal operation this pin features high impedance. If a feedback failure is detected (PFC_OK > 2.5 V & INV+40 mV < PFC_OK) the pin is asserted high. Normally, this pin is used to stop the operation of the DC-DC converter supplied by the PFC preregulator by invoking a latched disable of its PWM controller. If not used, the pin is left floating.

Pin 9 (PWM_STOP): Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.8 V on the RUN pin (#10) the voltage on the pin is pulled to ground. Normally, this pin is used to temporarily stop the

operation of the DC-DC converter supplied by the PFC preregulator by disabling its PWM controller. A typical use of this function is brownout protection in systems where the PFC preregulator is the master stage. If not used, the pin is left floating.

Pin 12 (GND). This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When layouting the printed circuit board, these two paths should run separately.

Pin 13 (GD) is the output of the driver. The pin is able to drive an external MOSFET with a 600 mA source and an 800 mA sink capability.

The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc. To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the L6563S is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (@ Isink = 2 mA), with $V_{cc} > V_{CC_ON}$. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET used for this purpose.

Pin 14 (Vcc) is the supply of the device. This pin is externally connected to the startup circuit (usually one resistor connected to the rectified mains) and to the self-supply circuit.

Whatever the configuration of the self-supply system, a capacitor is connected between this pin and ground.

To start the L6563S, the voltage must exceed the startup threshold (12 V typ.). Below this value the device does not work and consumes less than 90 µA (typ.) from Vcc. This allows the use of high value startup resistors (in the hundreds kΩ), which reduces power consumption and optimizes system efficiency at low load, especially in wide range mains applications.

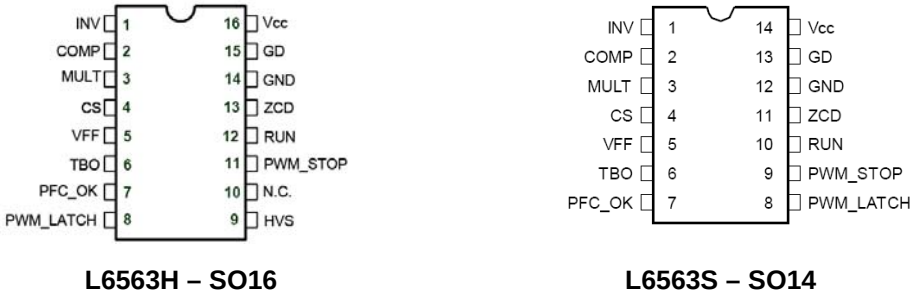
When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 6 mA.

The device keeps on working as long as the supply voltage is over the UVLO threshold (13 V max). If the Vcc voltage exceeds 22.5 V an internal Zener diode, 20 mA rated, is activated in order to clamp the voltage. Please remember that during normal operation the internal zener does not have to clamp the voltage, because in that case the power consumption of the device increases considerably and its junction temperature increases too. The suggested operating condition for safe operation of the device is below the minimum clamping voltage of the pin.

5 L6563H: high voltage startup transition mode PFC

The L6563H is a new current-mode PFC controller operating in transition mode (TM) which embeds the same features existing in the L6563S with the addition of a high voltage startup. Package and pin-out are different as shown in *Figure 21*. Pin function is the same, in this paragraph a detailed description of the HV startup system is given.

Figure 21. L6563H and L6563S pin-out comparison

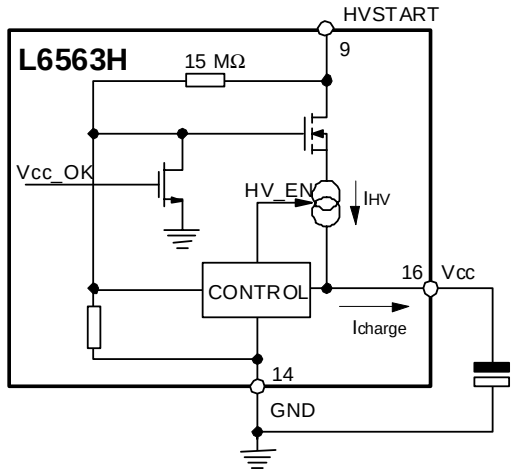


L6563H – SO16 **L6563S – SO14**

Figure 22 shows the internal schematic of the high-voltage startup generator. It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 M resistor, with a temperature compensated current generator connected to its source.

The HV generator is physically located on a separate chip, made with BCD off-line technology able to withstand 700 V, controlled by a low-voltage chip, where all of the control functions reside.

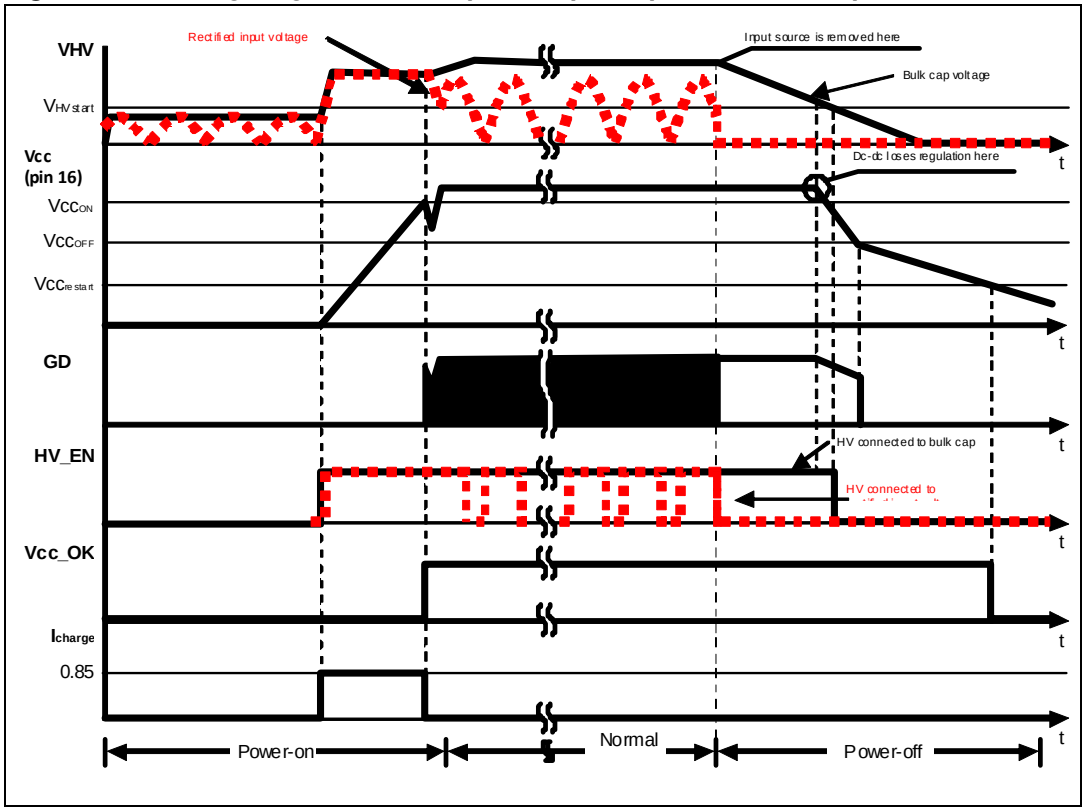
Figure 22. High-voltage startup generator: internal schematic



With reference to the timing diagram of *Figure 23*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This

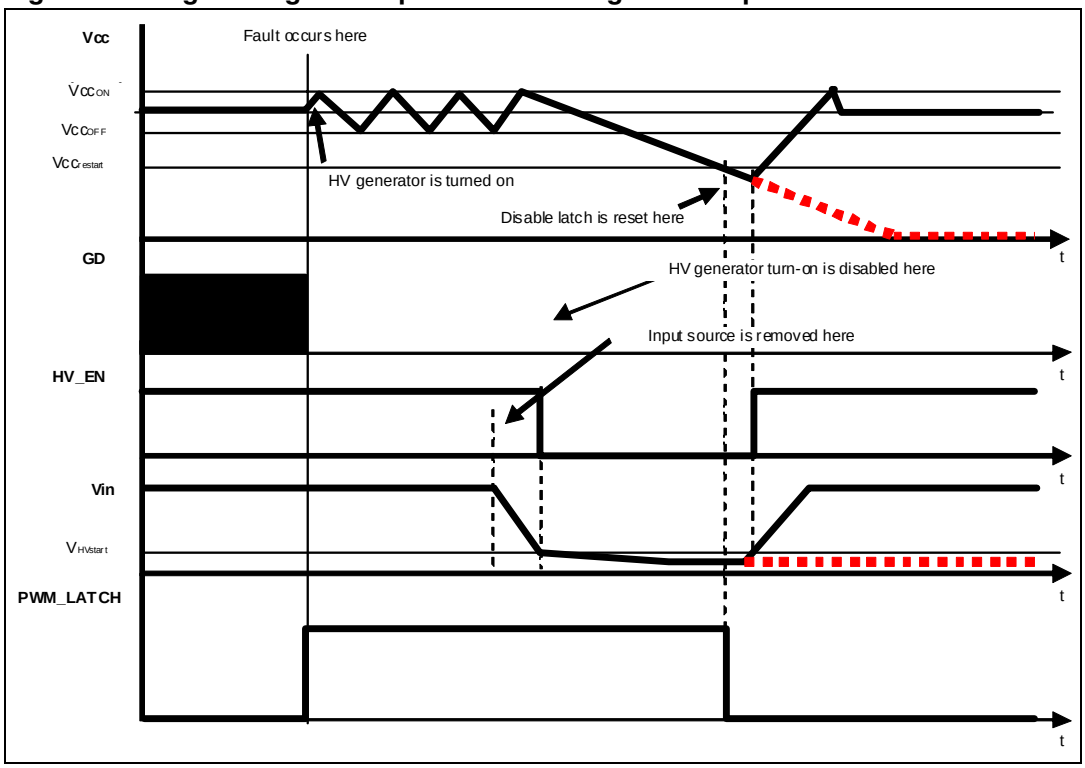
current, minus the device's consumption, charges the bypass capacitor connected from pin Vcc (*6*) to ground and makes its voltage rise almost linearly.

Figure 23. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the startup threshold (12V typ.) the low-voltage chip starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (we assume that it is made with an auxiliary winding in the transformer of the cascaded DC-DC converter and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 M resistor (10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard startup circuit made with external dropping resistors. At converter power-down the DC-DC converter loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc then drops and stops IC activity as it falls below the UVLO threshold (9.5 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold $V_{CCrestart}$ located at about 6 V. The HV generator can now restart. However, if Vin < $V_{HVstart}$, HV_EN is de-asserted too and the HV generator is disabled. This prevents the converter's restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used. If the device detects a fault due to feedback failure the pin PWM_LATCH is asserted high (see *Feedback failure protection* section for more details) and, in order to keep alive this signal to be provided to the DC-DC converter, the internal $V_{CCrestart}$ is brought up to over the V_{CCOff} (Turn-off threshold).

Figure 24. High-voltage startup behavior during latch-off protection



As a result, shown in *Figure 24*, the voltage at pin Vcc, oscillates between its turn-on and turn-off thresholds until the HV bus is recycled and drops below the startup threshold of the HV generator. The high voltage startup circuitry is capable of guaranteeing a safe behavior in case of a short circuit present on the DC-DC output when the Vcc of both controllers are generated by the same auxiliary winding.

Figure 25. High-voltage startup managing the DC-DC output short circuit

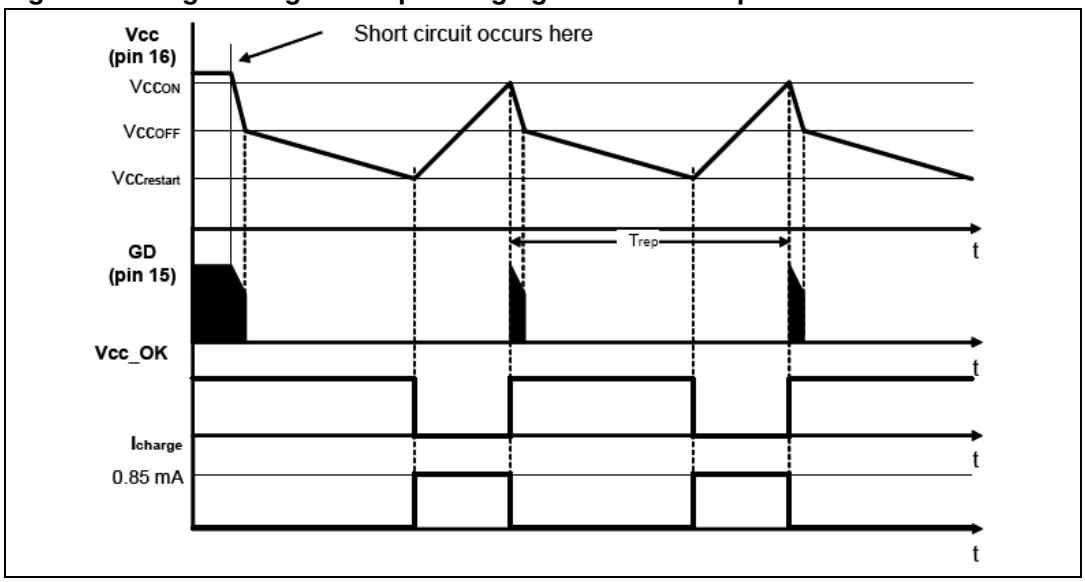


Figure 25 shows how the PFC manages the Vcc cycling and the associated power transfer.

At short circuit the auxiliary circuit is no longer able to sustain the Vcc which starts dropping; reaching its V_{CCOFF} threshold the IC stops switching, reduces consumption and drops more until the $V_{CCrestart}$ threshold is tripped. Now, the high voltage startup generator restarts and when the Vcc crosses its turn-on threshold again the IC starts switching. In this manner the power is transferred from mains to PFC output only during a short time for each Trep cycle.

6 Design example using the L6563S-FOT PFC Excel® spreadsheet

An Excel spreadsheet has been developed to allow a quick and easy design of a boost PFC preregulator using the STMicroelectronics' L6563S controller or the L6563H version, operating in FOT mode. As shown in *Figure 21* the package and the pin-out are different but most of the functions are the same and therefore they can be calculated in the same way. *Figure 26* and *Figure 27* show the first sheet filled with the input design data used in *Section 4.1 on page 9*.

Figure 26. Excel spreadsheet design specification input table

Design Specs:	Parameter	Value	Unit [ ]
Mains Voltage Range	VacMin	90	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	400	W
Max. Output Low Frequency Ripple	Δ Vout	10	Vpk-pk
Holdup Capability	Thold	20	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Max. Switching Frequency @ Vac min (on line voltage sinusoid peak):	fmax	80	kHz
Expected Efficiency	η	90	%
Expected Power Factor	PF	0.99	---
Max inductor current ripple to peak ratio (@VACmin,Pout_max)	Kr	0.34	---
Maximum Ambient Temperature	Tambx	50	°C

Figure 27. Other design data

Other Design Data:	Parameter	Value	Unit [ ]
Maximum Magnetic Flux Density	Bmax	0.25	T
Ripple Voltage Coefficient	r	0.1	---

The tool is able to generate a complete parts list of the PFC schematic represented in *Figure 28* or *Figure 29*, including the power dissipation calculation of the main components.

Figure 28. Excel spreadsheet FOT PFC using the L6563S (SO14-black pin out) schematic

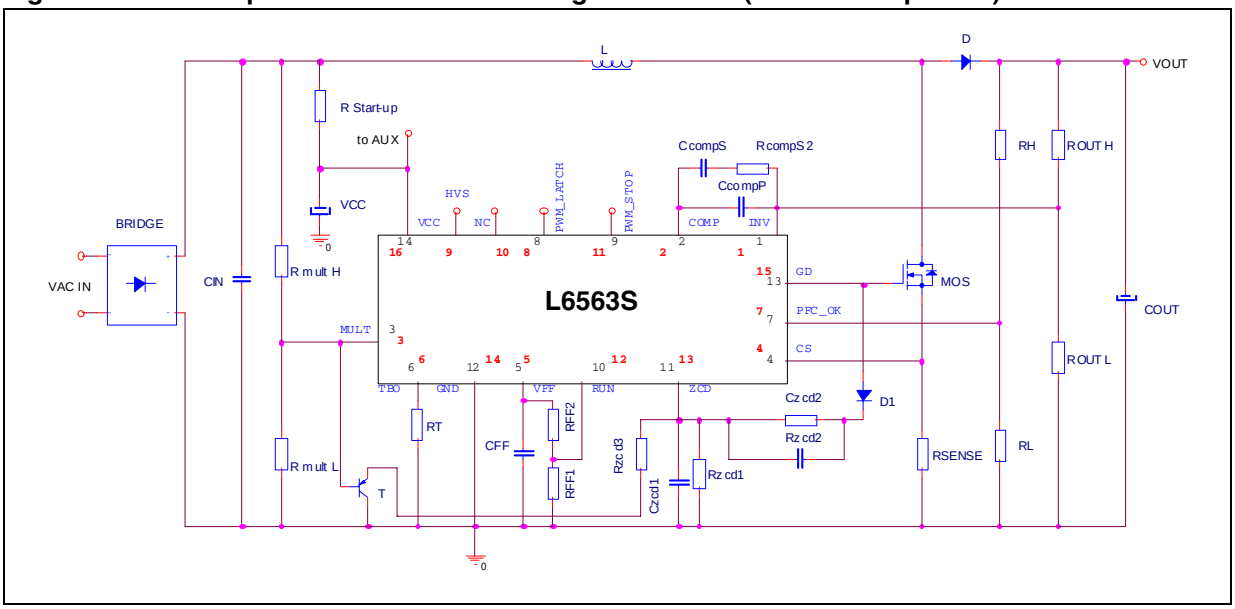
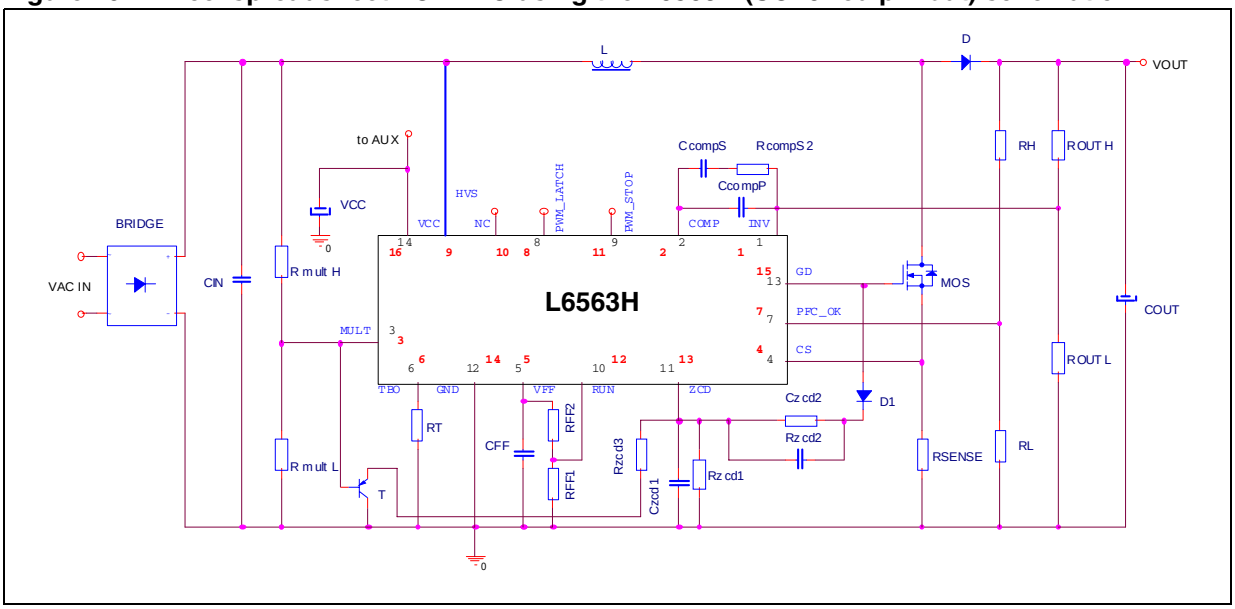


Figure 29. Excel spreadsheet FOT PFC using the L6563H (SO16-red pin out) schematic



The bill of materials in *Figure 30* is automatically compiled by the Excel spreadsheet. It summarizes all selected components and some salient data.

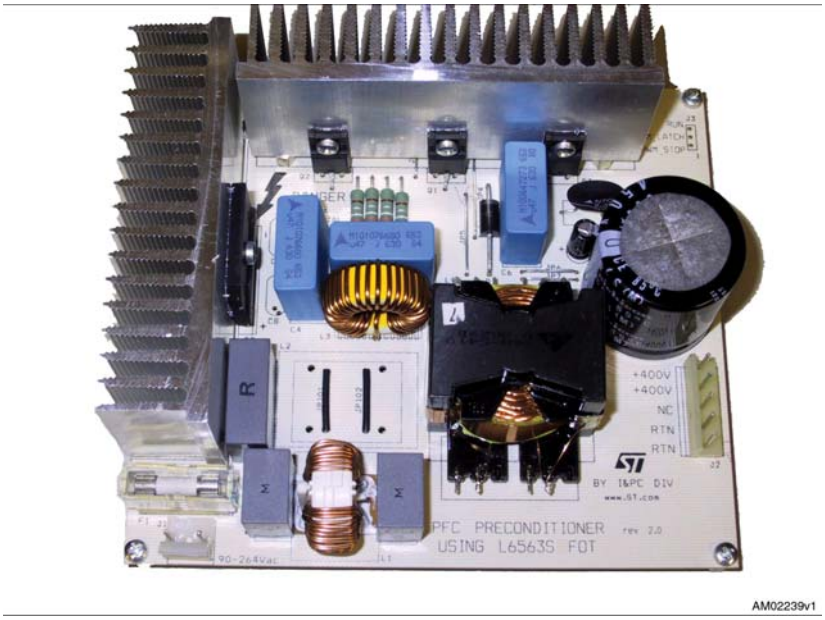
Figure 30. Excel spreadsheet BOM

400 W FOT PFC BASED ON L6563S/H
BILL OF MATERIAL

		Selected Value	Unit [ ]
BRIDGE RECTIFIER	*D15XB60*		
MOSFET P/N	*2 x STP12NM50PF*		
DIODE P/N	*STTH8R06*		
Inductor	*L*	*500*	*µH*
Max peak Inductor current	*Ilpkx*	*9.67*	*A*
Sense resistor	*Rsx*	*0.12*	*Ω*
Power dissipation	*Ps*	*2.14*	*W*
INPUT Capacitor	*Cin*	*1*	*µF*
OUTPUT Capacitor	*Cout*	*330*	*µF*
Pin3 - MULT Divider	*Rmult L*	*51*	*kΩ*
	Rmult H	*6600*	*kΩ*
ZCD FOT circuit	*Rzcd1*	*15*	*kΩ*
	Rzcd2	*1*	*kΩ*
	Rzcd3	*1.5*	*kΩ*
	Czcd1	*220*	*pF*
	Czcd2	*100*	*pF*
Diode P/N	*1N4148*		
pnp-BJT P/N	*BC857C*		
Feedback Divider	*RoutH*	*3000*	*kΩ*
	RoutL	*18.8*	*kΩ*
Output divider for PFC_OK	*RL*	*51*	*kΩ*
	RH	*8800*	*kΩ*
Compensation Network	*CcompP*	*100*	*nF*
	CcompS	*1000*	*nF*
	RcompS	*56*	*kΩ*
Voltage Feedforward	*CFF*	*1000*	*nF*
	RFF1	*1000*	*kΩ*
	RFF2	*56*	*kΩ*
IC Controller	*L6563S/H*		

In AN2994 (400 W FOT-controlled PFC preregulator with the L6563S), an evaluation board based on the transition-mode PFC controller L6563S is described and presents the results of its bench evaluation.

Figure 31. L6563S 400W FOT PFC demonstration board (p/n EVL6563S-400W)



7 Reference

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2. “Current mode control”, Venable Technical Paper #5, www.venableind.com
3. “Fixed-off-time control of PFC preregulators”, 10th european conference on power electronics and applications, EPE2003, Toulouse, France, paper 382
4. “L6563S, transition-mode PFC controller”, datasheet, www.st.com
5. “Design fixed-off-time-controlled PFC preregulators with the L6562”, AN1792
6. “400W FOT-controlled PFC preregulator with the L6563”, AN2485
7. “A systematic approach to frequency compensation of the voltage loop in boost PFC pre-regulator”, Abstract
8. “400 W FOT-controlled PFC preregulator with the L6563S”, AN2994

8 Revision history

Table 1. Document revision history

Date	Revision	Changes
10-Aug-2010	1	Initial release
01-Dec-2010	2	Updated *Chapter 4.3.7 on page 20*
09-Feb-2011	3	Updated: *Figure 11 on page 20*

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